REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

2. The allowability resides in the overall structure of the device as clamed in claim 10, and at least in part because claim 10 recites: " A cooling system for devices comprising power semiconductor components, the power semiconductor components being arranged on printed circuit boards along with non-power type semiconductor components, the printed circuit boards arranged in plug-in contact strips of a superordinate circuit carrier, the cooling system comprising: *a cooling plate mounted in a pivotable manner, via a tilting mechanism extending from an edge of the cooling plate to a tilting axis on a plug-in contact strip* in a region of one of the power semiconductor components, and which can be pivoted about the tilting axis which extends parallel to the plug-in contact strip, and *a cooling grid structure fitted on edges of the cooling plat*e and projecting in directions parallel to the plug-in contact strip; the cooling plate having a first mounting and maintenance position pivoted away from the power semiconductor component, and a second cooling and operating position wherein *the cooling plate is pressed directly onto and covers only the power semiconductor component while the cooling grid structure does not contact or cover the power semiconductor device, but covers only the remaining non-power semiconductor components* arranged on the printed circuit board adjacent to the power semiconductor component." (emphasis added). The aforementioned limitations, in combination with all remaining limitations of

claim 10, are believed to render the claim and all claims dependent therefrom (claims 11, 14-17, 30 and 34-37) patentable over the art of record.

The allowability further resides in the overall structure of the device as clamed in claim 18, and at least in part because claim 18 recites: "A power semiconductor device comprising: at least one printed circuit board arranged in one of a plurality of plug-in contact strips of a superordinate circuit carrier and having at least one power semiconductor component positioned thereon and a plurality of other semiconductor components arranged adjacent thereto; *a cooling plate mounted in a pivotable manner, via a tilting mechanism extending from I an edge of the cooling plate, to a tilting axis on the plug-in contact strip* in a region of the at least one of power semiconductor component and configured to be pivoted about the tilting axis via the tilting mechanism, wherein the tilting axis extends parallel to the plug-in contact strip; and *a cooling grid structure fitted on and extending from edges of the cooling plate*, the cooling plate having a first mounting and maintenance position pivoted away from the power semiconductor component, and a second cooling and operating position wherein *the cooling plate is pressed directly onto and covers only the power semiconductor component while the cooling grid structure does not contact or cover the power semiconductor component but covers at least a portion of only the plurality of other semiconductor components*." (emphasis added). The aforementioned limitations, in combination with all remaining limitations of claim 18, are believed to render the claim

and all claims dependent therefrom (claims 19, 22-25 and 31-32) patentable over the art of record.

The allowability further resides in the overall structure of the device as clamed in claim 26, and at least in part because claim 26 recites: "A method for cooling a device having power semiconductor components, the method comprising: *mounting pivotable cooling plates via tilting mechanisms extending from edges of the cooling plates to tilting axes extending along plug-in contact strips* of a superordinate circuit carrier, the cooling plates being in a mounting and maintenance position and having *a cooling grid structure fitted on and extending from edges thereof*; fitting printed circuit boards into the plug-in contact strips, the printed circuit boards having at least one power semiconductor component positioned thereon and a plurality of other semiconductor components arranged adjacent thereto…*pivoting the cooling plates about the tilting axes from the mounting and maintenance position into a cooling or operating position wherein the cooling plates are held directly in contact with a corresponding power semiconductor component of a corresponding printed circuit board while the cooling grid structure does not contact or cover the power semiconductor components but covers only the plurality of other semiconductor components adjacent thereto*; orienting a device generating a cooling air stream…and providing the cooling air stream during operation of the power semiconductor components in the event of a critical temperature of the power semiconductor components being reached." (emphasis added). The aforementioned

limitations, in combination with all remaining limitations of claim 26, are believed to render the claim patentable over the art of record.

The allowability further resides in the overall structure of the device as clamed in claim 27, and at least in part because claim 27 recites: “A cooling system for devices comprising at least one power semiconductor component, the power semiconductor component being arranged, along with a plurality of other semiconductor components, on a printed circuit board arranged in a plug-in contact strip of a superordinate circuit carrier, the cooling system comprising: *a cooling plate mounted in a pivotable manner, via a tilting mechanism extending from an edge of the cooling plate, to a tilting axis extending along the plug-in contact strip* in a region of the at least one power semiconductor component, the cooling plate having *a cooling grid structure fitted on and extending from edges thereof*; means for pivoting the cooling plate about the tilting axis, which is parallel to the plug-in contact strip, between a first mounting and maintenance position wherein the cooling plate is away from the power semiconductor component, and a second cooling and operating position wherein *the cooling plate is pressed directly onto the power semiconductor component while the cooling grid structure is positioned so as to not contact or cover the power semiconductor component*." (emphasis added). The aforementioned limitations, in combination with all remaining limitations of claim 27, are believed to render the claim and all claims dependent therefrom (claims 28, 33, 38 and 39) patentable over the art of record.

None of the references cited during prosecution of the instant application (including newly cited references to Gates et al. (US 7,079,396), Yasufuku et al. (US 6,890,202), Ali et al. (US 6,362,966), Duesman et al. (US 6,031,727) and Funari et al. (US 5,109,318)), either taken alone or in combination, is believed to render the present invention unpatentable as claimed. It is believed that the prior art does not teach or suggest a cooling system for printed circuit boards comprising a cooling plate arranged in a pivotable manner via a tilting mechanism to a tilt axis of plug in contact strips on a superordinate carrier with a cooling grid structure extending from the cooling plate edges, wherein the cooling plate directly contacts a power semiconductor while the cooling grid contacts other semiconductors components.

Furthermore, the Examiner has performed inventor and assignee names search for possible double patenting issues. No documents with conflicting claims have been identified.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRADLEY H. THOMAS whose telephone number is (571)272-9089. The examiner can normally be reached on 7:00am - 3:30pm (Eastern).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayprakash N. Gandhi can be reached on 571-272-3740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BHT

/Jayprakash N Gandhi/
Supervisory Patent Examiner, Art Unit 2835